

Final Expansion 3 Registers

All registers are initialized to zero at power on.

Mode register \$9C02

m	m	m	b	b	b	b	b
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mmm – Mode

000	Start mode
010	Super ROM mode
100	RAM 1 mode
110	RAM 2 mode
101	Super RAM mode
011	RAM/ROM
001	Flash mode

bbbbbb – Bank or other mode parameter

Start Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	-	-	-	-
BLK1	EEPROM Bank 0	-	RAM Bank 1	-
BLK2	EEPROM Bank 0	-	RAM Bank 1	-
BLK3	EEPROM Bank 0	-	RAM Bank 1	-
BLK5	EEPROM Bank 0	-	RAM Bank 1	-

?Lock bit? - write to BLK5 = clear, read from BLK5 = set

Super ROM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	?	-	?	-
BLK1	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK2	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK3	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK5	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-

RAM 1 Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	?RAM Bank 0?	-	?RAM Bank 0?	b_0 – write enable
BLK1	RAM Bank 1	-	RAM	$b_1 - 0$ = Bank 1, 1 = Bank 2
BLK2	RAM Bank 1	-	RAM	$b_2 - 0$ = Bank 1, 1 = Bank 2
BLK3	RAM Bank 1	-	RAM	$b_3 - 0$ = Bank 1, 1 = Bank 2
BLK5	RAM Bank 1	-	RAM	$b_4 - 0$ = Bank 1, 1 = Bank 2

RAM 2 Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	?RAM Bank 0?	b_0 – write enable
BLK1	RAM	$b_1 - 0$ = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK2	RAM	$b_2 - 0$ = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK3	RAM	$b_3 - 0$ = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK5	RAM	$b_4 - 0$ = Bank 1, 1 = Bank 2	RAM Bank 1	-

Super RAM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0?	-
BLK1	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK2	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK3	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK5	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$

RAM/ROM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	?RAM Bank 0?	b_0 – write enable
BLK1	RAM/EEPROM	$b_1 - 0$ = RAM Bank 1, 1 = EEPROM Bank 0	RAM Bank 1	-
BLK2	RAM/EEPROM	$b_2 - 0$ = RAM Bank 1, 1 = EEPROM Bank 0	RAM Bank 1	-
BLK3	RAM/EEPROM	$b_3 - 0$ = RAM Bank 1, 1 = EEPROM Bank 0	RAM Bank 1	-
BLK5	RAM/EEPROM	$b_4 - 0$ = RAM Bank 1, 1 = EEPROM Bank 0	RAM Bank 1	-

Flash Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	?	-	?	-
BLK1	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK2	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK3	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK5	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$

Resource register \$9C03

e	a	b	5	3	2	1	r
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e – Register disable

0	Registers enabled
1	Registers disabled

ab – ?Address lines?

a	A14
b	A13

5 – BLK5 disable

0	BLK5 enabled
1	BLK5 disabled

5 – BLK3 disable

0	BLK3 enabled
1	BLK3 disabled

5 – BLK2 disable

0	BLK2 enabled
1	BLK2 disabled

5 – BLK1 disable

0	BLK1 enabled
1	BLK1 disabled

5 – RAM1,2,3 disable

0	RAM1,2,3 enabled
1	RAM1,2,3 disabled